REMARKS

Claims 1-46 are currently pending in the application. Claims 1-33 and 35-46 were rejected. Claim 34 was objected to.

The Examiner rejected claims 1-33 and 35-46 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Publication No. 2002/0049824 A1 (Wilson). The rejection is respectfully traversed.

Wilson describes a multi-processor computer architecture having a distributed shared memory. The system includes a plurality of uniform memory access (UMA) cells 100 interconnected by an interconnect 20. Each UMA cell includes a processor 102 and a memory 104 which includes a memory controller 106. Each memory controller 106 includes a so-called "cache of history counter" (CofHC) 108. Each entry in CofHC 108 represents a page (indicated by page address field 112) in the associated memory 104 and includes a plurality of counters (e.g., 114-120 of Fig. 2). Each counter for a given entry tracks a different metric for the corresponding page. For example, each of counters 114, 115, and 116 corresponds to one of the other UMA's (e.g., 200, 300, etc.) in the system, and tracks the accesses by the processor in the corresponding UMA to the memory page in memory 104 represented by the entry. Migration counter 118 is incremented upon each migration of the page. Write counter 120 is incremented for each write to the page. By tracking these metrics, the system can determine (e.g., using the decision tree 250 of Fig. 3) whether there is a more efficient memory location for a given page in memory. See paragraphs [0023]-[0030]. Significantly, none of the counters described by Wilson determine or track transaction latency.

By contrast, claim 1 of the present invention recites "a latency counter operable to generate a latency count for each of selected" memory transactions. That is, the recited latency counter maintains a count which is representative of the length of time (e.g., as measured in clock cycles) required for such transaction.

Claim 1 also recites "a plurality of histogram counters," each of which is "operable to count selected ones of the latency counts corresponding to an associated latency range." That is, each histogram counter tracks the number of transaction latencies (as determined by the latency counter) which fall within a particular latency range, e.g., 400 to 600 clock cycles. See the present application from page 32, line 20 to page 33, line 21, and Fig. 14.

Wilson neither describes nor suggests the determination or tracking of transaction latency as recited in claim 1 of the present application. Wilson does note that the information collected by the CoHC counters may be used to determine whether a particular memory page should be replicated or migrated to a different memory location which, in turn, may result in improvements in system latency (see paragraph [0030]). However, Wilson does not discuss how or even whether such latency improvements are determined. In any case, latency measurements are clearly not performed or tracked using the CoHC counters or any of the other components of the Wilson's system.

In view of the foregoing, claim 1 is believed to be allowable over the Wilson reference for at least the reasons discussed. For similar reasons, claims 22 and 38 are also believed to be allowable. In addition, all of the claims dependent on claims 1, 22, and 38 are believed to be allowable for at least the reasons discussed.

The Applicants respectfully acknowledge the Examiner's indication of allowable subject matter in claim 34. However, in view of the foregoing, claim 34 is believed to be allowable without amendment.

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CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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